FAR

PRIMARIUS

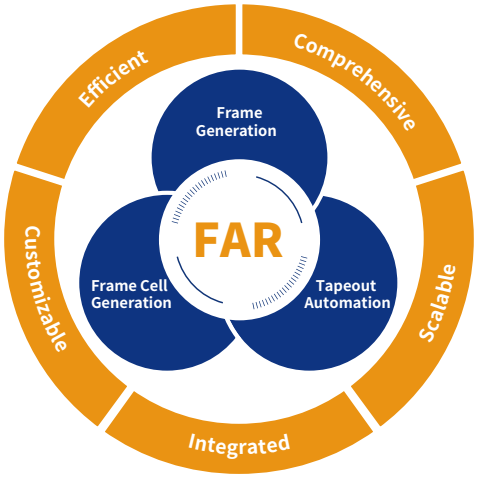
Reticle Automated Design Platform

Introduction

Primarius FAR is a comprehensive foundry tapeout automation platform designed for the efficient generation of frames and frame cells. It streamlines the tapeout process in semiconductor manufacturing by offering robust automation and customizable features tailored to meet diverse project needs.

FAR ensures high precision in generating layout patterns and frames, essential for semiconductor integrity. The platform handles projects of various scales and integrates with existing tools for seamless workflow. By automating key steps, FAR minimizes human error and provides comprehensive documentation for quality control.

FAR accelerates the tapeout process, critical for competitive time-to-market, and improves quality by generating precise monitor patterns and alignment marks. This efficiency lowers production costs and fosters innovation, enabling design teams to focus on developing advanced semiconductor technologies.



Specifications

- Technology Nodes
  FinFET 14nm, 28nm and above
- Frame Cells Types
  OVL, CDBar, Litho Alignment marks, OCD, Thickness PAD, Thrupitch, OPC pattern, etc.
- Frame Types
  Single chip, multiple products wafer(MPW)
- Outer scribeline Types
  Zero overlap, full overlap, alternate half overlap and partial overlap
- Information Extraction
  Chip center coordinates, frame cell center coordinates, label positions and GDS information

Key Advantages

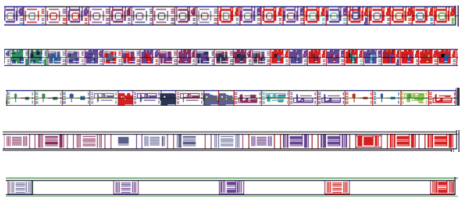
- One-Stop Design Platform
  Foundry tapeout one-stop platform including frame GDS, frame cells GDS generation and tapeout automation
- Flexible User Interface
  Support floorplan editor, debug placement, wafer map, and customizable functions user interfaces
- Tapeout Automation
  Product tapeout information automatically extracted for Foundry and maskshop
- Frame Cells Generation
  Support frame cells generation including inline monitor patterns, litho alignment marks, etc
- Comprehensive Inspection
  Support chips, frame cells and chips, frame cells overlap check and customized checking
- Customization
  Support customized functions to optimize customer tapeout flow

Applications

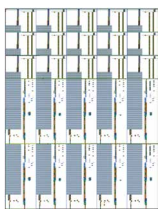
- Foundry tapeout
- Fabless chip information extraction

Application Examples

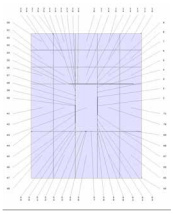
Frame Cells Generation



Frame GDS Files



Tapeout Documents



Wafer Map